FPGA Real-time Linear Frequency Modulated Continuous Wave Signal Processing

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INTRODUCTION

The system developed in this research is part of the backend signal processing system for the Capacitive Micro-machined Ultrasound Doppler Sensor developed at the Microscale Sensors and Systems Lab [1]. The sensor is intended for small scale mobile navigation systems[1]. Consequently, the velocity and distance have be determined in real-time for navigation to be possible.

The sensor's transmitter propagates frequency modulated continuous wave (FMCW) ultrasound with a center frequency of 180kHz, and a bandwidth of 20 Hz, and the receiver detects the reflected waves.

The signal processing system (basic schematic shown in Figure 1) has a two part scheme that contains an analog demodulation and filtering circuit and an FPGA system that detects input frequencies and computes the distance and velocity of the reflecting obstacle.

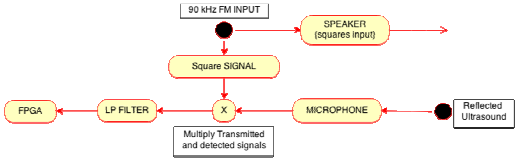


Figure 1: Signal Processing Scheme

Because of the transmitter's dynamics, the output frequency of the speaker is the square of the driving frequency . Therefore, an output of 180kHz is driven by 90kHz.

OBJECTIVES

The focus of this research was to design an FPGA signal processing system that detects the two major tones from the low-pass filter output, and use the frequency values to compute the velocity and distance of the reflecting obstacle.

The FPGA development platform used in this system is a National Instruments sbRIO 9631 FPGA board and its associated programming language – Labview FPGA. The sbRIO 9631 has 32 16-bit ±10V analog inputs, 1M gate reconfigurable I/O for custom timing, and a 266 MHz processor. This FPGA is also part of the DaNI FPGA robotic platform; thus, it is a convenient platform to test the navigation application of the sensor and its signal processing system.

SIGNAL PROCESSING

The FPGA signal processing scheme, entails reading in a data sample (of size 2^n) from the FPGA, through the Direct Memory Access queue (DMA FIFO) to the real-time machine. The FIFO is restarted every cycle so that the FIFO buffer collects new data. In the real-time machine, operations which are not time intensive (like Fast Fourier Transforms - FFT) are conducted, and the required tones are extracted, based on the amplitude the detected frequencies in the input signal.

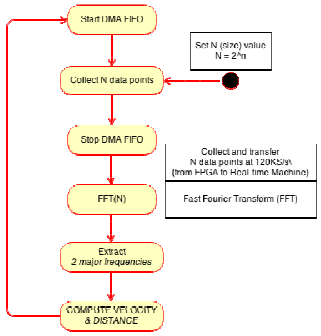


Figure 2: Signal Processing Flow Diagram

EXPECTED INPUT:

The low-pass filter is expected to output a two-tone signal, for example Figure 3 shows a spectral power plot and FPGA input signal with tones A and B.

SIMULATED INPUT:

To simulate the input , a summing amplifier was used to add two signals from two waveform generators. With this simulation, the robustness of the system could be easily tested by varying the generators' signals

SAMPLING FREQUENCY AND RESOLUTION

The sampling period is 8µs (125 kS/s), this is mainly limited by the Analog to Digital Converter, since the FPGA can operate at 40 MHz. The number of samples collected is configured to always equal 2^n so that the FFT algorithms are most efficient for sample sizes of 2^n. Because the sampling frequency is fixed the sample size affects the resolution of the FFT output.

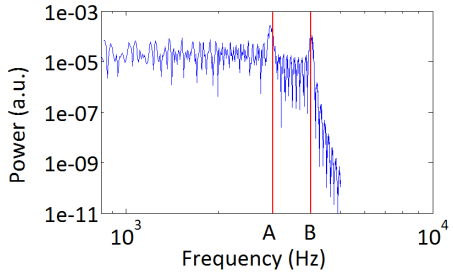


Figure 3: Expected Input Signal (contains two major tones)

The frequency resolution (Δf) can be calculated using Equation 1.

$$\Delta f = \frac{1}{125\,000 * 2^n} \qquad (1)$$

However, as the sample size increases, the system results frequency will be reduces.

VELOCITY AND DISTANCE CALCULATION

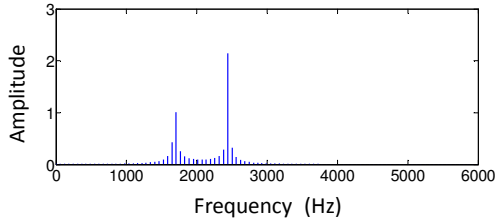
The velocity (V) and distance (D) can be calculated using Equation 2 and 3 [3], respectively.

$$V = \left(\frac{f_A - f_B}{2}\right)\left(\frac{c}{f_c}\right), D = \left(\frac{f_A + f_B}{2}\right)\left(\frac{c}{4 + f_b + f_m}\right) \qquad (2,3)$$

Where c is the speed of sound, f_A and f_B are the two tone frequencies in the FPGA signal input, and f_C is the ultrasound carrier frequency (180 kHz). f_b and f_m are the Low Pass Filter bandwidth, and ultrasound frequency modulation, respectively.

RESULTS

From a simulated input of 2.13kHz and 1.7kHz signals , and a sample size of 2^{11}, the system detects 1709 Hz and 2136Hz, with a resolution of 61Hz. The system updates 6 times per second. The velocity and distance are evaluated to be 5.812m/s and 0.0048m, respectively. Figure 4 is the displayed spectral density plot from the Labview front panel.



The front panel also displays the input signal.

FUTURE WORK

The next phase of the research entails testing the complete system (i.e. sensor, analog circuit, and FPGA system). Apart from velocity and distance measurement, the system will also be test for potential applications in material classification based on the differences in the materials' ultrasound reflection coefficient.

Potentially, the sampling frequency can be significantly improved if a better Analog to Digital Converter (ADC) is used. For this reason, the Texas Instruments' ADS5560 - 16-bit 40MSPS Low Power ADC will be tested as well.

REFERENCES

[1] M. Shin, R. D. White, P. DeBitetto and J. S. Krause, "Acoustic Doppler Velocity Measurement System using Capacitive Micromachined Ultrasound Transducer Array Technology," *Journal of the Acoustical Society of America,* vol. 134, no. 2, pp. 1011-1020, 2013.

[2] M. Shin, Z. Zhao, P. DeBitetto and R. White, "Micromachined ultrasonic Doppler velocity sensor using nickel on glass transducers," Sensors and Actuators A: Physical, vol. 208, pp. 37-49, 1 February 2014.

[3] V. Issakov, Microwave circuits for 24 GHz automotive radar in silicon-based technologies, Neubiberg: Springer, 2010.